

Notice of References Cited	Application/Control No. 09/008,531		Applicant(s)/Patent Under Examination RHODES, HOWARD E.	
	Examiner Kurt M. Eaton		Art Unit 2823	Page 1 of 1

U.S. PATENT DOCUMENTS

*	A	DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS	DOCUMENT SOURCE **	
							APS	OTHER
<input type="checkbox"/>	A	US005484741A	Jan. 1996	Bergemont	437	43	<input checked="" type="checkbox"/>	<input type="checkbox"/>
<input type="checkbox"/>	B	US005668053A	Sep. 1997	Akimoto	438	625	<input checked="" type="checkbox"/>	<input type="checkbox"/>
<input type="checkbox"/>	C	US005312769A	May. 1994	Matsuo et al.	437	52	<input checked="" type="checkbox"/>	<input type="checkbox"/>
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FOREIGN PATENT DOCUMENTS

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NON-PATENT DOCUMENTS

*	A	DOCUMENT (Including Author, Title Date, Source, and Pertinent Pages)	DOCUMENT SOURCE **	
			APS	OTHER
<input type="checkbox"/>	U	Wolf et al., "Silicon Processing for the VLSI Era; Volume 1 - Process Technology", Lattice Press, 1986, pages 547-54.	<input type="checkbox"/>	<input checked="" type="checkbox"/>
<input type="checkbox"/>	V		<input type="checkbox"/>	<input type="checkbox"/>
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*A copy of this reference is not being furnished with this Office action. (See Manual of Patent Examining Procedure, Section 707.05(a).)

**APS encompasses any electronic search i.e. text, image, and Commercial Databases.

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